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Karen Cinq-Mars 6/15/04
(Signature & date)



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of _____ :

June 15 2004

Bruce B. Doris, et al _____ :

Group Art No: 2818

Serial No. 10/604,190 _____ :

Examiner: David Vu

Filed: 6/30/03 _____ :

IBM Corporation
Bldg. 300, Zip 482
2070 Route 52
Hopewell Junction, NY 12533

Title: HIGH PERFORMANCE CMOS
DEVICE STRUCTURES AND METHOD
OF MANUFACTURE _____ :

TITLE: HIGH PERFORMANCE CMOS DEVICE STRUCTURES AND METHOD OF
MANUFACTURE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

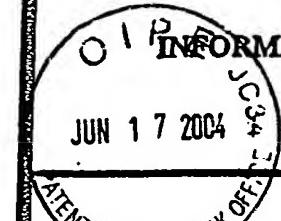
In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

If any fees are required for this submission, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Bruce B. Doris, et al.

By

Joseph P. Abate 6-15-04
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~~INFORMATION DISCLOSURE CITATION~~

(Use several sheets if necessary)

JUN 17 2004

Docket Number (Optional)
FIS920030152US1

Application Number
10/604,190

Bruce B. Doris, et al

Filing Date

6/30/03

Group Art Unit

2818

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER DOCUMENTS (*Including Author, Title, Date, Pertinent Pages, Etc.*)

	<p>Novel Locally Strained Channel Technique for High Performance 55nm CMOS K. Ota, et al. 2002 IEEE, 2.2.1-2.2.4, IEDM 27.</p> <p>Local Mechanical-Stress Control (LMC): A New Technique for CMOS - Performance Enhancement A. Shimizu, et al. 2001 IEEE, 19.4.1-19.4.4, IEDM 01-433</p> <p>Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design Shinya Ito, et al. 2000 IEEE, 10.7.1-10.7.4, IEDM 00-247</p> <p>A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System -on-a- Chip Applications F. Ootsuka, et al. 2000 IEEE, 23.5.1-23.5.4, IEDM 00-575</p>
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EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with ~~law~~ Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

2001-0001

Docket Number (Optional)
FIS920030152US1

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Applicant(s)

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U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER DOCUMENTS (*Including Author, Title, Date, Pertinent Pages, Etc.*)

NMOS Drive Current Reduction Caused by Transistor-Layout and Trench Isolation Induced Stress
Gregory Scott, et al. 1999 IEEE, 34.4.1-34.4.4, IEDM 99-827 .

Transconductance Enhancement in Deep Submicron Strained-Si n- MOSFETs
Kern (Ken) Rim, et al. 1998 IEEE, 26.8.1-26.8.4, IEDM 98-707

Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFET's
K. Rim, et al. 2002 IEEE, 98-99, 2002 Symposium On VLSI Technology Digest of Technical Papers

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